NEWS RELEASE

SYMPOSIUM REVEALS LATEST FINDINGS IN MICROELECTRONICS RELIABILITY

IRPS 2004 sees the largest submission of technical papers in the event's history.

PHOENIX, ARIZ. – April 25, 2004 – The 2004 International Reliability Physics Symposium (IRPS) reports the largest submission and acceptance of technical papers in its 42-year history of providing the latest developments in the reliability and performance of circuits and devices to the microelectronics industry.

The latest research on Cu/low k interconnects and novel transistor reliability findings will be featured at the 2004 IRPS, continuing its tradition of providing a forum for cutting-edge technology and research.

At this premier symposium for electronics reliability, researchers will be able to hear the authors discuss their findings in technical sessions, tutorials, workshops, hands-on equipment demonstrations and a poster session. Also continuing in its second year at IRPS is the Reliability Year in Review, which will bring attendees up to speed on the latest developments in this growing field. IRPS 2004 is being held from April 25 through April 29, 2004, at the Hyatt Regency Phoenix at Civic Plaza, Phoenix, Ariz.

"In our 42nd year, IRPS continues to explore the cutting edge of the state of the art in the microelectronics industry," said Bernie Pietrucha, IRPS 2004 General Chair. "The largest submission of technical papers in our history is certain to stir up some lively discussions at IRPS this year."

Technical Program Highlights

Solving Negative-Bias Temperature Instability (NBTI) on surface channel PMOS Transistors

Papers in the "Novel transistor reliability findings" plenary session discuss recent results of key wearout mechanisms (NBTI and Hot Carrier) for novel MOSFET structures and processes that can be potentially used in future state-of-the-art CMOS technologies.

The NBTI sensitivity of triple gate pMOSFETs is presented for the first time. Worst case NBTI degradation is observed and attributed to an enhanced interface states density increase along the (110) SiO_2/Si interface. ***Session 1.1: "Broad energy distribution of NBTI-induced interface states in P-MOSFETs with ultra-thin nitrided oxide," J.H. Stathis et al, IBM.*** The other NBTI paper sheds some light into the microscopic nature of the NBTI damage in pMOSFETs with ultra thin nitrided gate oxides. In particular, the measured difference in interface state energy distribution indicates a different nature of the NBTI damage between nitrided vs. pure SiO_2 gate oxides. ***Session 1.2: "Negative bias temperature instability in triple gate transistors," S. Maeda et al, Samsung Electronics.***

Two of the papers give new insights into the physics of the Hot Carrier damage of n-MOSFET with Si-Ge strained layers and alternatively with HfSiON gate dielectric. In both cases it is found that the worst case stress condition is Vg=Vd. ***Session 1.3: "Investigation of hot carrier effects in n-MISFETs with HfSiON gate dielectric," M. Takayanagi et al, Toshiba; Session 1.4: "Hot carrier degradation in novel strained-Si nMOSFETs," M.F. Lu et al, UMC.***

All four papers given in this session clearly suggest that the future state of the art CMOS technologies will present new reliability challenges.

Interconnects:

Stress-induced voiding and its interaction with low-k dielectrics is highlighted at this year's IRPS. Two abstracts describe different aspects of dual-damascene Cu via voiding. A featured abstract submitted by engineers from AMD, shows that voiding under an isolated via gets progressively worse when lower-k materials are integrated. Using finite element (FE) analysis and relating voiding tendencies to a critical stress threshold, it is shown that lower-k materials exhibit more pronounced void nucleation tendencies, despite possessing lower overall thermo-mechanical stress. They also discuss how void nucleation exhibits line width dependence through careful FE modeling. ***Session 4B.3: "Stress modeling of Cu/low-K BEOL -application to stress migration," C. J. Zhai et al, AMD.***

Another key abstract, submitted by engineers from Chartered Semiconductor and Nanyang Technological University, addresses the issue of voiding within and at the bottom of a Cu via. Such voids are shown to be generated through small defects that arise during process and integration. These defects can grow during thermal stressing and can be further exacerbated by Cu metal contraction upon cooling. Process improvements can substantially enhance via robustness. However, it is also found that further degradation in via voiding occurs when lower-k dielectric is used. Thus, further process improvements may be necessary to ensure required stress migration robustness. ***Session 4B.4: "Stress-induced voiding in multi-level Copper/low-k interconnects," Y.K. Lim et al., Chartered Semiconductor Mfg. Ltd.& Nanyang Technological Univ.***

SER Performance:

SER performance issues are addressed in "***Session 6A.2 Process impact on SRAM alpha-particle SEU performance:"—Y.Z. Xu et al., Cypress Semiconductor.*** In this paper, the impact of many process variations are quantified on the SER performance of 0.15um SRAM, concluding that the most effective technology tweak is to add additional capacitance to sensitive nodes. Comparisons of the SER of Bulk and SOI SRAM in the 180,130 and 90nm technology nodes from lifetests (unaccelerated), accelerating testing and simulation, showing good agreement between the methods, is explored in ***Session 6A.3: "Neutron-induced soft-error in logic device using quasi-monoenergetic neutron beam," S. Yamamoto, et al., Renesas Technology Corp.***

Back-End Integration:

The reliability of a stacked via chain stressed under various thermal cycle conditions is one topic under review in the back-end integration sessions. The chain consists of Cu Dual Damascene metalization with SiLK (trademark of Dow Chemical) as the organic low-k dielectric. Failure analysis indicates that cracks form in the Cu vias during thermal cycle stress. Due to the presence of two failure modes, the thermal cycle statistical behavior is described by a bimodal lognormal failure distribution. The thermal cycle lifetime exhibits a strong dependence on the temperature range and a rather weak dependence on the maximum temperature in the cycle. Evidence of a threshold temperature range below which thermal cycle fails should not occur is also reported.

Session 21b.2: "Thermal Cycle Reliability of stacked Via Structures with copper Metalization and an Organic Low-K Dielectric," R.G. Filippi et al., IBM.

Failure Analysis:

A quantitative application of thermal/laser based analytical techniques such as TIUA and OBIRCH in the first paper that extends Thermal Laser Stimulation (TLS) from binary fault isolation techniques to quantitative measurement techniques that can be used to extract reliability data from semiconductor devices. ***Session 6C.4, "Thermal laser stimulation of active devices in silicon - a quantitative FET parameter investigation," C. Boit et al., TUB Berlin University of Technology.***

A review of the hardware used for optical non-destructive VLSI structural analysis technique based on ultrasound generation and detection by picosecond laser pulses as well as initial data is provided in ***Session 6C.7 "Structural Analysis of integrated circuits using scanning laser ultrasonics,"G. Andriamonje et al.***

Other Sessions

In addition to these highlighted areas, IRPS 2004 will also include sessions on Design Practices, ESD, Future CMOS, Latch Up, Memory, MEMS, Products and Circuits, General Reliability, RF/MMIC Reliability and High K and SIO_2 Dielectrics.

About IRPS

For over 40 years, IRPS has been one of the leading meetings for engineers in the area of electronic component reliability. IRPS promotes the comprehension of reliability and performance of integrated circuits and microelectronic assemblies through an improved understanding of failure mechanisms in the user's environment. Originally started in the early 1960's by the military and aerospace community, IRPS is now sponsored by IEEE Reliability Society and IEEE Electron Devices Society. All accepted IRPS papers will appear in the symposium proceedings publication, as well as on the Virtual IRPS DVD-ROM, which is available now for the previous 2003 IRPS.

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